## CO-SIMULATION OF VERILOG/PLI AND SYSTEM C MODULES USING REMOTE PROCEDURE CALL

### **REMARKS**

This responds to the Office Action dated October 19, 2005.

Claim 19 is hereby amended and no claims are canceled or added; as a result, claims 1-30 remain pending in this application.

## Claim 19 Amendment

Claim 19 is amended to correct a typographical error regarding claim dependency. Claim 19 was previously dependent upon itself. Claim 19 is correct to depend from independent claim 11. As such, this amendment is not made in light of the rejection. Reconsideration and allowance of claim 19 are respectfully requested.

# §102 Rejection of the Claims

Claims 1-20 were rejected under 35 U.S.C. § 102(e) for anticipation by Hekmatpour (U.S. Pub. No. 2002/01569292)(hereinafter "Hekmatpour"). Detailed traversals of the rejections are provided as follows:

#### CLAIM 1

Applicant respectfully traverses the rejection on several grounds. Among other things, Hekmatpour fails to teach or suggest the subject matter of claims 1-20. In traversing the rejections, Applicant does not address the question of whether Hekmatpour can be removed from consideration and does not waive that option by making this traversal.

For example, it is respectfully submitted that the cited portions of Hekmatpour fails to provide, among other things, using a remote procedure call (RPC) to transfer process control to a server module that models behavior of a component of the electronic system, as set forth in claim 1. The Office Action refers to Hekmatpour paragraphs [0058]-[0062]; however Applicant is unable to locate such a teaching therein.

Hekmatpour further fails to contemplate "controllably advancing simulation time" as set forth in claim 1. The Office Action refers to paragraph [0077] which recites:

Dkt: 303.741US1

[0077] Thus, all members of the design tem have access to the current sate of the design and the continuously updated design repository, and changes made by any one member is instantly and simultaneously seen by all of the members. In this manner, the design flow does not grind to a halt while one designer finishes a particular task, such as the simulation task.

There is no mention of "controllably advancing simulation time" in this paragraph. Applicant is further unable to locate a relevant teach or suggestion to do so.

Reconsideration and allowance of claim 1 are respectfully requested.

## CLAIMS 2-10

Claims 2-10 depend ultimately on claim 1 and are believed allowable for at least the reasons set forth for claim 1. Additionally, the cited portion of the cited reference is believed to fail to teach or suggest Verilog/PLI as recited in claim 2 and SystemC as recited in claim 3. The cited portions of the cited reference also fail to provide the RPC using the TCP or UDP protocols as transport layer protocols as set forth in claims 4 and 5. Additionally, it is believed that there is no teaching or suggestion in the cited portion of Hekmatpour of suspending operation of the server module as set forth in claim 7. The cited portion of the cited reference also is believed to lack a teaching or suggestion of advancing simulation time by one cycle of a clock signal as set forth in claim 9.

Reconsideration and allowance of claims 2-10 are respectfully requested.

## CLAIM 11

Applicant respectfully traverses the rejection on several grounds. Among other things, Hekmatpour fails to teach or suggest the subject matter of claims 1-20. In traversing the rejections, Applicant does not address the question of whether Hekmatpour can be removed from consideration and does not waive that option by making this traversal.

For example, it is respectfully submitted that the cited portions of Hekmatpour fails to provide, among other things, using a remote procedure call (RPC) to transfer process control to a server module that models behavior of a component of the electronic system, as set forth in claim 11. The Office Action refers to Hekmatpour paragraphs [0058]-[0062]; however Applicant is unable to locate such a teaching therein.

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Hekmatpour further fails to contemplate "controllably advancing simulation time" as set forth in claim 11. The Office Action refers to paragraph [0077] which recites:

[0077] Thus, all members of the design tem have access to the current sate of the design and the continuously updated design repository, and changes made by any one member is instantly and simultaneously seen by all of the members. In this manner, the design flow does not grind to a halt while one designer finishes a particular task, such as the simulation task.

There is no mention of "controllably advancing simulation time" in this paragraph. Applicant is further unable to locate a relevant teach or suggestion to do so.

Reconsideration and allowance of claim 11 are respectfully requested.

#### **CLAIMS 12-20**

Claims 12-20 depend ultimately on claim 11 and are believed allowable for at least the reasons set forth for claim 11. Additionally, the cited portion of the cited reference is believed to fail to teach or suggest Verilog/PLI as recited in claim 12 and SystemC as recited in claim 13. The cited portions of the cited reference also fail to provide the RPC using the TCP or UDP protocols as transport layer protocols as set forth in claims 14 and 15. Additionally, it is believed that there is no teaching or suggestion in the cited portion of Hekmatpour of suspending operation of the server module as set forth in claim 17. The cited portion of the cited reference also is believed to lack a teaching or suggestion of advancing simulation time by one cycle of a clock signal as set forth in claim 19.

Reconsideration and allowance of claims 12-20 are respectfully requested.

Thus, Applicant respectfully submits that claims 1-20 are patentable over Hekmatpour. Withdrawal of the Section 102(e) rejections and allowance of the claims is earnestly requested.

#### Allowed Subject Matter

Applicant acknowledges the allowance of claims 21-30.

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# **CONCLUSION**

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612) 373-6912 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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